WHAT IS CLAIMED IS:

1. A multichip module comprising:

a first chip having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface, each of said bonding pads operable for bonding a wire;

a second chip having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface, each of said bonding pads operable for bonding a wire;

a first attach layer having an area equal to an area of said second chip bottom surface for coupling said first chip and said second chip, said first attach layer having a thickness to provide electrical disconnection of said first chip wire bonds and said second chip, said first attach layer is applied to said second chip bottom surface prior to coupling said first chip and said second chip.

2. The multichip module of Claim 1, wherein said electrical disconnection is provided as a gap between said first chip wire bonds and said second chip, and wherein said gap is approximately 10 μm.

3. The multichip module of Claim 1, wherein said first attach layer is a thermosetting material, wherein said thermosetting material is pliable for coupling said first chip and said second chip such that said thermosetting material conforms to said first chip wire bond.

4. The multichip module of Claim 1, wherein said first chip top and bottom surfaces and said second chip top and bottom surfaces have equal areas.

5. The multichip module of Claim 1, wherein said first chip and said second chip have a stacked arrangement such that said first chip bonding pads are covered from above by said second chip.

6. The multichip module of Claim 1 further including a second attach layer having an area equal to said second chip bottom surface area and disposed between said first attach layer and said second chip bottom surface, said second attach layer being an insulating material having a thickness cooperable with said first attach layer to provide electrical disconnection of said first chip wire bonds and said second chip.

7. The multichip module of Claim 6, wherein said first attach layer is a thermosetting material, wherein said thermosetting material is pliable for coupling said first chip

and said second chip such that said thermosetting material conforms to said first chip wire bond and said second attach layer is silicon dioxide.

8. The multichip module of Claim 6, wherein said electrical disconnection is provided as a gap between said first chip wire bonds and said second chip, and wherein said gap is approximately equal to said second attach layer thickness.

9. The multichip module of Claim 6, wherein said second attach layer thickness is approximately 1 μm.

10. The multichip module of Claim 6, wherein said first chip top and bottom surfaces and said second chip top and bottom surfaces have equal areas, and wherein said first and second chips are stacked such that said first chip bonding pads are covered from above by said second chip.

11. A method of arranging a plurality of integrated chips in a multichip module, comprising:

providing a first chip having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface;

bonding a wire to each of said bonding pads;

providing a second chip having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface;

applying a first attach layer having an area equal to an area of said second chip bottom surface for coupling said first chip and said second chip, said first attach layer having a thickness to provide electrical disconnection of said first chip wire bonds and said second chip; and

coupling said first chip and second chip, wherein said second chip bottom surface is coupled to said first chip top surface via said first attach layer.

12. The method of Claim 11, wherein said first attach layer is applied to said second chip bottom surface prior to coupling said first chip and said second chip.

13. The method of Claim 11, wherein said first attach layer is a thermosetting material, wherein said thermosetting material is pliable for coupling said first chip and said second chip such that said thermosetting material conforms to said first chip wire bond.

14. The method of Claim 11 further including providing said first chip top and bottom surfaces and said second chip top and bottom surfaces with equal areas.

15. The method of Claim 11 further including coupling said first chip and said second chip to provide a stacked arrangement such that said first chip bonding pads are covered from above by said second chip.

16. The method of Claim 11 further providing a second attach layer having an area equal to said second chip bottom surface area and disposed between said first attach layer and said second chip bottom surface, said second attach layer being an insulating material having a thickness cooperable with said first attach layer to provide electrical disconnection of said first chip wire bonds and said second chip.

17. The method of Claim 16, wherein said electrical disconnection is provided as a gap between said first chip wire bonds and said second chip, and wherein said gap is approximately equal to said second attach layer thickness.

18. The method of Claim 17, wherein said second attach layer thickness is approximately 1 μm.

19. The method of Claim 16, wherein said first attach layer is a thermosetting material, wherein said thermosetting material is pliable for coupling said first chip and said second chip such that said thermosetting material conforms to said first chip wire bond.

20. The method of Claim 16 further including providing said first chip top and bottom surfaces and said second chip top and bottom surfaces with equal areas and coupling said first chip and said second chip to provide a stacked arrangement such that said first chip bonding pads are covered from above by said second chip.